WHAT IS CLAIMED IS:

1. A thin film transistor array substrate comprising:

an insulating substrate;

a first metallic pattern formed on said insulting substrate;

an insulating film provided on said first metallic pattern;

a semiconductor pattern provided on said insulating film; and

a second metallic pattern provided on said semiconductor pattern;

wherein said second metallic pattern is surrounded by said semiconductor pattern.

2. The thin film transistor array substrate according to claim 1, wherein at the source electrode part in a pixel region, a part of the semiconductor pattern surrounding the source electrode exists only on the first metallic pattern.

3. A thin film transistor array substrate comprising:

an insulating substrate;

a gate line formed on said insulating substrate;

a gate insulating film provided on said gate line;

a semiconductor layer provided on said gate insulating film;

a source line, a source electrode and a drain electrode provided on said semiconductor layer;

and

a pixel electrode formed on said drain electrode;

wherein said source line, said source electrode and said drain electrode are surrounded by said semiconductor layer;

wherein said pixel electrode is directly in contact with at least a portion of said drain electrode.

4. A thin film transistor array substrate comprising:

an insulating substrate;

a gate line formed on said insulating substrate;

a gate insulating film provided on said gate line;

a semiconductor layer provided on said gate insulating film;

a source line, a source electrode and a drain electrode provided on said semiconductor layer;

an inter-layer insulating film formed on said source line, said source electrode and said drain electrode; and

a pixel electrode formed on said inter-layer insulating film;

wherein said source line, said source electrode and said drain electrode are surrounded by said semiconductor layer;

wherein said inter-layer insulating film is provided with a first contact hole, a second contact hole and a third contact hole, said first contact hole penetrating said inter-layer insulating film to reach said drain electrode, said second contact hole extending to said source line through said inter-layer insulating film, said third contact hole extending to said gate line through said gate insulating film and said inter-layer insulating film; and

wherein said first contact hole, said second contact hole and said third contact hole are covered with a pattern made of a material of said pixel electrode.

5. The thin film transistor array substrate according to claim 4, wherein at the source electrode part in a pixel region, a part of the semiconductor pattern surrounding the source electrode exists only on the gate line.

6. Method for manufacturing a thin film transistor array substrate comprising steps of:

a first photolithography and etching step for forming a gate line;

depositing a gate insulating film, a semiconductor film, an ohmic contact film and a first metallic thin film;

a second photolithography step for forming a resist pattern of a source line, a source electrode, and a drain electrode;

forming a region of said resit pattern serving as a semiconductor active layer in the thin film transistor in such a manner that thickness of said resist pattern in at least said region serving as a semiconductor active layer is smaller than that in said source line, said source electrode and said drain electrode in the second photolithography process after depositing a second metallic film;

etching said second metallic film to form the source line, the source electrode and the drain electrode;

removing the resist in the region serving as a semiconductor active layer and etching said second metallic film to remove said second metallic film on said region serving as a semiconductor active layer, removing said ohmic contact film on said region serving as a semiconductor active layer;

a third photolithography and etching step of patterning the

gate insulating film for forming a contact hole extending to the gate line;

depositing a conducting film; and

a fourth photolithography and etching step of forming a pixel electrode in such a manner that said pixel electrode is connected with said drain electrode.

7. Method for manufacturing a thin film transistor array substrate comprising steps of:

a first photolithography and etching step for forming a gate line;

depositing a gate insulating film, a semiconductor film, an ohmic contact film and a first metallic thin film;

a second photolithography step for forming a resist pattern of a source line, a source electrode, and a drain electrode;

forming a region of said resit pattern serving as a semiconductor active layer in the thin film transistor in such a manner that thickness of said resist pattern in at least said region serving as a semiconductor active layer is smaller than that in said source line, said source electrode and said drain electrode in the second photolithography process after depositing a second metallic film;

etching said second metallic film to form the source line, the source electrode and the drain electrode;

removing the resist in the region serving as a semiconductor active layer and etching said second metallic film to remove said second metallic film on said region serving as a semiconductor active layer, removing said ohmic contact film on said region serving as a semiconductor active layer;

a third photolithography and etching step of patterning the gate insulating film for forming a contact hole extending to the gate line;

depositing a conducting film; and

a fourth photolithography and etching step of forming a pixel electrode in such a manner that said pixel electrode is connected with said drain electrode, forming a source terminal in such a manner that said source terminal is connected with said source line, forming a gate terminal in such a manner that said gate terminal is connected with said gate line.

8. Method for manufacturing a thin film transistor array substrate comprising steps of:

a first photolithography and etching step for forming a gate line;

depositing a gate insulating film, a semiconductor film, an ohmic contact film and a first metallic thin film;

a second photolithography step for forming a resist pattern of a source line, a source electrode, and a drain electrode;

forming a region of said resit pattern serving as a semiconductor active layer in the thin film transistor in such a manner that thickness of said resist pattern in at least said region serving as a semiconductor active layer is smaller than that in said source line, said source electrode and said drain electrode in the second photolithography process after depositing a second metallic film;

etching said second metallic film to form the source line, the source electrode and the drain electrode;

thinning the resist to remove the resist only in the region

serving as a semiconductor active layer and etching said second metallic film to remove said second metallic film on said region serving as a semiconductor active layer, removing said ohmic contact film on said region serving as a semiconductor active layer;

depositing an inter-layer insulating film;

a third photolithography and etching step of patterning said gate insulating film and said inter-layer insulating film to form a first contact hole extending to said drain electrode, a second contact hole extending to said source line and a third contact hole extending to said gate line;

depositing a conducting film; and

a fourth photolithography and etching step of forming a pixel electrode in such a manner that said pixel electrode is connected with said drain electrode via said first contact hole, forming a source terminal in such a manner that said source terminal is connected with said source line via said second contact hole, forming a gate terminal in such a manner that said gate terminal is connected with said gate line via said third contact hole.

9. Method for manufacturing a thin film transistor array substrate comprising steps of:

a first photolithography and etching step for forming a gate line and a conversion line for a source line;

depositing a gate insulating film, a semiconductor film, an ohmic contact film and a first metallic thin film;

a second photolithography step for forming a resist pattern of a source line, a source electrode, and a drain electrode;

forming a region of said resit pattern serving as a semiconductor active layer in the thin film transistor in such a manner that thickness of said resist pattern in at least said region serving as a semiconductor active layer is smaller than that in said source line, said source electrode and said drain electrode in the second photolithography process after depositing a second metallic film;

etching said second metallic film to form the source line, the source electrode and the drain electrode;

removing the resist in the region serving as a semiconductor active layer and etching said second metallic film to remove said second metallic film on said region serving as a semiconductor active layer, removing said ohmic contact film on said region serving as a semiconductor active layer;

a third photolithography and etching step of patterning said gate insulating film to form a first contact hole extending to said drain electrode, a second contact hole extending to said source line, a third contact hole extending to said gate line, a fourth contact hole extending to gate line material of said conversion line and a fifth contact hole extending to the source line;

depositing a conducting film; and

a fourth photolithography and etching step of forming a pixel electrode in such a manner that said pixel electrode is connected with said drain electrode via said first contact hole, forming a source terminal in such a manner that said source terminal is connected with said source line via said second, fourth and fifth contact hole, forming a gate terminal in such a manner that said gate terminal is connected with said gate line via said third contact hole.

10. Method for manufacturing a thin film transistor array substrate comprising steps of:

a first photolithography and etching step for forming a gate line and a conversion line for a source line formed of a first metallic film;

depositing a gate insulating film, a semiconductor film, an ohmic contact film and a first metallic thin film;

a second photolithography step for forming a resist pattern of a source line, a source electrode, and a drain electrode;

forming a region of said resit pattern serving as a semiconductor active layer in the thin film transistor in such a manner that thickness of said resist pattern in at least said region serving as a semiconductor active layer is smaller than that in said source line, said source electrode and said drain electrode in the second photolithography process after depositing a second metallic film;

etching said second metallic film to form the source line, the source electrode and the drain electrode;

removing the resist in the region serving as a semiconductor active layer and etching said second metallic film to remove said second metallic film on said region serving as a semiconductor active layer, removing said ohmic contact film on said region serving as a semiconductor active layer;

depositing an inter-layer insulating film;

a third photolithography and etching step of patterning said gate insulating film and said inter-layer insulating film to form a first contact hole extending to said drain electrode, a second contact hole extending to said source line, a third contact hole extending to said gate line, a fourth contact hole extending to the first metallic film of said

conversion line for the source line and a fifth contact hole extending to said second metallic film;

depositing a conducting film; and

a fourth photolithography and etching step of forming a pixel electrode in such a manner that said pixel electrode is connected with said drain electrode via said first contact hole, forming a source terminal in such a manner that said source terminal is connected with said source line via said second, fourth and fifth contact hole, forming a gate terminal in such a manner that said gate terminal is connected with said gate line via said third contact hole.

11. A thin film transistor array for a liquid crystal display comprising:

a gate line/gate electrode comprising a transparent conductive layer and a metallic layer provided on said transparent conductive layer;

a pixel electrode defined by the same transparent conductive layer as said transparent conductive layer of said gate line/gate electrode; and

retaining capacitance electrode formed of the same material for an electrode as that for a source line, said retaining capacitance electrode being connected with said pixel electrode;

wherein said metallic layer provided on said gate line/gate electrode is removed from in a part serving as said pixel electrode.

12. A thin film transistor array for a liquid crystal display comprising:

a gate line/gate electrode and a common line, both of which comprise a transparent conductive layer and a metallic layer provided on said transparent conductive layer;

a pixel electrode defined by the same transparent conducive layer as said transparent conductive layer of said gate line/gate electrode; and

a retaining capacitance electrode formed of the same material for an electrode as that for a source line, said retaining capacitance being connected with pixel electrode;

wherein said metallic layer provided on said gate line/gate electrode is removed from in a part serving as said pixel electrode.

13. A thin film transistor array for a liquid crystal display comprising:

a gate line/gate electrode comprising a transparent conductive layer and a metallic layer provided on said transparent conductive layer;

a pixel electrode defined by the same transparent conductive layer as said transparent conductive layer of said gate line/gate electrode; and

retaining capacitance electrode formed of the same material for an electrode as that for a source line, said retaining capacitance electrode being connected with said pixel electrode;

wherein said metallic layer provided on said gate line/gate electrode is removed from in a part serving as said pixel electrode;

wherein at least a material for said source line located in a lowermost layer is the same material as that for said metallic layer of the

pixel electrode, when a material for said source line has a muti-layered structure or said source line per se has a multi-layered structure.

14. A thin film transistor array for a liquid crystal display comprising:

a gate line/gate electrode and a common line, both of which comprise a transparent conductive layer and a metallic layer provided on said transparent conductive layer;

a pixel electrode defined by the same transparent conductive layer as said transparent conductive layer of said gate line/gate electrode; and

retaining capacitance electrode formed of the same material for an electrode as that for a source line, said retaining capacitance electrode being connected with said pixel electrode;

wherein said metallic layer provided on said gate line/gate electrode is removed from in a part serving as said pixel electrode;

wherein at least a material for said source line located in a lowermost layer is the same material as that for said metallic layer of the pixel electrode, when a material for said source line has a muti-layered structure or said source line per se has a multi-layered structure

15. A thin film transistor array for a liquid crystal display comprising:

a gate line/gate electrode including at least two layers comprising a metallic layer and a transparent conductive layer, said metallic layer being formed on said transparent conductive layer;

a pixel electrode being formed by a transparent conductive

layer which is the same as said transparent conductive layer of said gate line/gate electrode;

a gate insulating film and a semiconductor layer being formed on at least said gate electrode;

source/drain electrodes being formed in such a manner as to contact with said semiconductor layer;

at least an n^+- Si layer of said semiconductor layer located between said source/drain electrodes being removed;

a retaining capacitance electrode which is formed of a same layer as that of said source line;

a retaining capacitance line including at least two layers comprising said metallic layer and said transparent conductive layer simultaneously formed with said gate line, wherein a retaining capacitance is formed in such a manner that said retaining capacitance electrode is opposed to said gate line via said gate insulating film;

at least said gate insulating film, said semiconductor layer, and said metallic layer of said pixel electrode being simultaneously formed with said gate line/gate electrode including at least two layers, which are located over a light transmitting portion are removed;

a part of said semiconductor layer being removed in order that adjacent source lines are not short-circuited with said semiconductor layer;

said gate insulating film having such a thickness right under said semiconductor layer is larger than that at any other part of said gate insulating film.

16. A thin film transistor array for a liquid crystal display

comprising:

a gate line/gate electrode and a common line including two layers comprising a metallic layer and a transparent conductive layer, said metallic layer being formed on said transparent conductive layer;

a pixel electrode being formed by a transparent conductive layer which is the same as said transparent conductive layer of said gate line/gate electrode;

a gate insulating film and a semiconductor layer being formed at least on said gate electrode;

a source/drain electrodes being formed in such a manner as to contact with said semiconductor layer;

at least an n^+- Si layer of said semiconductor layer being located between said source/drain electrodes is removed;

a retaining capacitance electrode, which is formed of a same layer as said source line, being connected with said pixel electrode;

a retaining capacitance line including at least two layers comprising metallic layer and said transparent conductive layer simultaneously formed with said gate line, wherein a retaining capacitance is formed in such a manner that said retaining capacitance electrode is opposed to said common line via said gate insulating film;

at least said gate insulating film, said semiconductor layer, and said metallic layer of said pixel electrode simultaneously formed with said gate line/gate electrode including at least two layers, which are located over a light transmitting portion being removed;

a part of said semiconductor layer being removed in order that adjacent source lines are not short-circuited with said semiconductor layer;

said gate insulating film has such a thickness right under said semiconductor layer being larger than that at any other part of said gate insulating film.

17. Method for manufacturing a TFT array of liquid crystal display comprising steps of:

depositing a gate electrode/gate line and a pixel electrode, each of said gate electrode/gate line and said pixel electrode including at least two layers comprising a transparent conductive layer and metallic layer provided on said transparent conductive layer, and subsequently etching said gate electrode/gate line and said pixel electrode using a photoresist having patterns corresponding to said gate electrode/gate line and said pixel electrode to form a predetermined patterns;

forming a gate insulating film and a semiconductor film;

exposing said pixel electrode by etching process using said photoresist having patterns;

removing said metallic layer having at least two layer in said exposed pixel electrode by etching process; and

forming a drain electrode, a source electrode, and a source line.

18. Method for manufacturing a TFT array of liquid crystal display comprising steps of:

depositing a gate electrode/gate line and a pixel electrode, each of said gate electrode/gate line and said pixel electrode including at least two layers comprising a transparent conductive layer and metallic layer provided on said transparent conductive layer, and subsequently

etching said gate electrode/gate line and said pixel electrode using a photoresist having a patterned shape corresponding to said gate electrode/gate line and said pixel electrode to form a predetermined patterns;

forming a gate insulating film and a semiconductor film;

exposing said pixel electrode by etching process using said photoresist having patterns;

forming a metallic layer for a drain electrode, a source electrode, and a source line;

etching said metallic layer using said photoresist having the the predetermined patterns to form said drain electrode, said source electrode, and said source line;

wherein said metallic layer in said exposed pixel electrode having at least two layers.

19. Method for manufacturing a TFT array of liquid crystal display comprising steps of:

depositing a gate electrode/gate line and a pixel electrode, each of said gate electrode/gate line and said pixel electrode including at least two layers comprising a transparent conductive layer and metallic layer provided on said transparent conductive layer, and subsequently etching said gate electrode/gate line and said pixel electrode using a photoresist having a patterned shape corresponding to said gate electrode/gate line and said pixel electrode to form a predetermined patterns;

forming a gate insulating film and a semiconductor film;

forming a region (A) where at least of a portion of said

photoresist corresponding to said semiconductor layer to be left has a thickness being larger than any other part of said photoresist, a region (C) where at least of a portion of said photoresist corresponding to a light transmitting part of said pixel electrode to be exposed is removed, and a region (B) where any parts other than said region (A) and said region (B) having a thickness smaller than that of said semiconductor layer;

etching said semiconductor layer and said gate insulating film using said photoresist having said thickness in each part to expose said pixel electrode;

removing at least said metallic layer located in upper side of said two layers in said exposed pixel electrode by etching process;

removing said photoresist in said region (B) from upper side while leaving said phoresist in said region (A);

removing said photoresit in any part other than that in said region (A); and

forming a source/drain electrodes.

20. Method for manufacturing a TFT array of liquid crystal display comprising steps of:

depositing a gate electrode/gate line, a pixel electrode and a common line, each of said gate electrode/gate line, said pixel electrode and said common line including at least two layers comprising a transparent conductive layer and a metallic layer provided on said transparent conductive layer;

etching said gate electrode/gate line, said pixel electrode and said common line using a photoresist having a patterned shape corresponding to said gate electrode/gate line, said pixel electrode and

said common line to form a predetermined pattern;

forming a gate insulating film and a semiconductor film;

forming a region (A) where at least of a portion of said photoresist corresponding to said semiconductor layer to be left has a thickness being larger than any other part of said photoresist, a region (C) where at least of a portion of said photoresist corresponding to a light transmitting part of said pixel electrode to be exposed is removed, and a region (B) where any parts other than said region (A) and said region (B) having a thickness smaller than that of said semiconductor layer;

etching said semiconductor layer and said gate insulating film using said photoresist having said thickness in each part to expose said pixel electrode;

removing at least said metallic layer located in upper side of said two layers in said exposed pixel electrode by etching process;

removing said photoresist in said region (B) from upper side while leaving said phoresist in said region (A);

removing said photoresit in any part other than that in said region (A); and

forming a source/drain electrodes.

21. Method for manufacturing a TFT array of liquid crystal display comprising steps of:

depositing a gate electrode/gate line and a pixel electrode, each of said gate electrode/gate line and said pixel electrode including at least two layers comprising a transparent conductive layer and metallic layer provided on said transparent conductive layer, and subsequently etching said gate electrode/gate line and said pixel electrode using a

photoresist having a predetermined patterned shape corresponding to said gate electrode/gate line and said pixel electrode to form a predetermined patterns;

forming a gate insulating film and a semiconductor film;

forming a region (A) where at least of a portion of said photoresist corresponding to said semiconductor layer to be left has a thickness being larger than any other part of said photoresist, a region (C) where at least of a portion of said photoresist corresponding to a light transmitting part of said pixel electrode to be exposed is removed, and a region (B) where any parts other than said region (A) and said region (B) having a thickness smaller than that of said semiconductor layer;

etching said semiconductor layer and said gate insulating film using said photoresist having said thickness in each part to expose said pixel electrode;

removing said photoresist in said region (B) from upper side while leaving said phoresist in said region (A);

removing said photoresit in any part other than that in said region (A);

forming a source/drain electrode made of the same metallic material as that used for an upper layer of said two layers of said gate line; and

removing said source/drain electrode by etching process, while removing said metallic layer located in said upper layer of said two layers of said exposed pixel electrode by etching process.

22. TFT array substrate for a liquid crystal comprising:

source lines and gate lines which are formed in matrix;

a pixel electrode for applying voltage to a liquid crystal and thin film transistors, said pixel electrode being provided in each of parts in which said source lines are intersected with said gate lines, said pixel electrode being protected by a passivation film;

a gate electrode;

a gate insulating film formed on said gate electrode;

a semiconductor layer film provided on said gate insulating film on a region of said gate electrode, said semiconductor layer being formed in such a manner as to contact with said gate insulating film;

a source electrode, a source line and a drain electrode, each of said source electrode, said source line and said drain electrode including at least two layers comprising a transparent conductive film and a metallic film provided on said transparent conductive layer, said transparent conductive film being formed in such a manner as to partially contact with said semiconductor layer;

wherein said drain electrode is connected with said pixel electrode by said transparent conductive layer per se;

wherein said passivation film, and said metallic film and said passivation film which are located on said light transmitting part of said pixel electrode are removed.

23. Method for manufacturing TFT array substrate for a liquid crystal display comprising steps of:

forming at least a gate insulating film and a semiconductor layer on a gate electrode;

forming a region (A) in a photoresist having a large thickness to be left as a semiconductor layer, a region (C) where a photoresist is

removed to expose a gate line, and a region (B) other than said region (A) in a photoresist having a thickness smaller than said region (A);

removing at least gate insulating film and said semiconductor layer which are located on said gate line by subjecting said gate insulating film and said semiconductor layer to etching process using a photoresist having different thickness to partially expose said gate electrode;

reducing the thickness of said photoresist, and subsequently removing said photoresist in said region (B) while leaving said photoresist in said region (A); and

removing said semiconductor layer located in a part other than said region (A).

24. Method for manufacturing a TFT array substrate comprising steps of:

depositing a conductive material for a gate electrode/gate line;

etching said deposited conductive material using a photoresist having patterned shape corresponding to said gate electrode and said gate line to form a predetermined patterns;

forming a gate insulating film and a semiconductor layer;

forming a region (A) in a photoresist having a large thickness to be left as a semiconductor layer, a region (C) where a photoresist is removed to expose a gate line, and a region (B) other than said region (A) in a photoresist having a thickness smaller than said region (A);

removing at least gate insulating film and said semiconductor layer which are located on said gate line by subjecting

said gate insulating film and said semiconductor layer to etching process using a photoresist having the above-mentioned shape to expose at least a part of said gate electrode;

removing said photoresist in said region (B) while leaving said photoresist in said region (A);

removing said semiconductor layer located in a part other than said region (A);

forming a source/drain electrodes using a photoresist having a patterned shape corresponding to said source/drain electrodes in a transparent conductive layer formed in such a manner as to partially contact with said semiconductor layer and a metallic layer formed on said transparent conductive layer;

forming a passivation film;

removing at least a light transmitting part of said passivation film over a pixel electrode; and

forming a pixel electrode by removing said metallic layer on said transparent conductive layer from said removed passivation film formed on said pixel electrode.

25. The thin film transistor array substrate according to any one of claims 1, 12, 13, 14, 15, 16 or 22, wherein a semiconductor pattern is formed to have a region surrounding a thin film transistor and a region surrounding a source electrode and at least a part of a source line, and at the source electrode part in a pixel region, a part of the semiconductor pattern surrounding the source electrode exists only on a gate line.

26. The method of manufacturing a thin film transistor array substrate according to any one of claims 17, 18, 19, 20, 21, 23 or 24 wherein a semiconductor pattern is formed to have a region surrounding a thin film transistor and a region surrounding a source electrode and at least a part of a source line, and at the source electrode part in a pixel region, said semiconductor pattern is formed so that a part of the semiconductor pattern surrounding the source electrode exists only on a gate line.

27. A liquid crystal display apparatus comprising a thin film transistor array substrate manufactured by the method according to any one of claims 6, 7, 8, 9, 10, 17, 18, 19, 20, 21, 23 or 24.

28. A liquid crystal display apparatus comprising a thin film transistor array substrate according to any one of claims 1, 2, 3, 4, 5, 8, 11, 12, 13, 14, 15, 16 or 22.